

February 1990 Revised November 1999

100393

Low Power 9-Bit ECL-to-TTL Translator with Latches

General Description

The 100393 is a 9-bit translator for converting F100K logic levels to TTL logic levels. A LOW on the latch enable (LE) latches the data at the input state. A HIGH on the LE makes the latches transparent. A HIGH on either the ECL or TTL output enable (OE ECL or OE TTL), holds the outputs in a high impedance state.

The 100393 is designed with TTL, 64 mA outputs for Bus Driving capability. All ECL inputs have 50 $k\Omega$ pull-down resistors. When the inputs are either unconnected or at the same potential, the outputs will go LOW.

Features

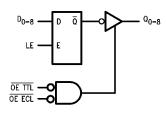
- 64 mA I_{OL} drive capability
- 2000V ESD protection
- -4.2V to -5.7V operating range
- Latched outputs
- TTL outputs

Ordering Code:

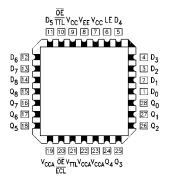
Order Number	Package Number	Package Description
100393QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

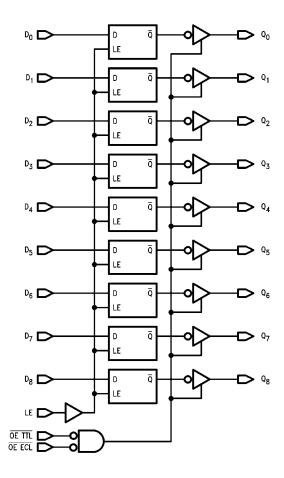
Pin Names	Description					
D ₀ –D ₈	Data Inputs (ECL)					
D ₀ –D ₈ Q ₀ –Q ₈	Data Outputs (TTL)					
LE	Latch Enable Input (ECL)					
OE TTL	Output Enable (TTL)					
OE ECL	Output Enable (ECL)					

Truth Table

	Inputs						
OE TTL	OE TTL OE ECL		D _N	Q _N			
L	L	Н	L	L			
L	L L		Н	Н			
L	L	L	Х	Latched			
Н	Х	Х	X	Z			
Х	Н	Х	X	Z			

- H = HIGH Voltage Level L = LOW Voltage Level X = Don't Care Z = High Impedance

Logic Diagram



Absolute Maximum Ratings(Note 1)

-65°C to +150°C Storage Temperature (T_{STG}) +150°C Maximum Junction Temperature (T_J) Case Temperature under Bias (T_C) 0°C to +85°C V_{EE} Pin Potential to Ground Pin -7.0V to +0.5VV_{TTL} Pin Potential to Ground Pin -0.5V to +6.0V ECL Input Voltage (DC) V_{EE} to +0.5V TTL Input Voltage -0.5V to +7.0V Output Current (DC Output HIGH) +130 mA ESD (Note 2) ≥2000V

Recommended Operating Conditions

Case Temperature ($T_{\rm C}$) 0°C to +85°C Supply Voltage

V_{EE} -5.7V to -4.2V V_{TTL} +4.5V to +5.5V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

DC Electrical Characteristics (Note 3)

 $V_{EE} = -4.2 V \ to \ -5.7 V; \ V_{CC} = V_{CCA} = GND, \ V_{TTL} = +4.5 V \ to \ +5.5 V, \ T_{C} = 0 ^{\circ}C \ to \ +85 ^{\circ}C$

Symbol	ol Parameter		Min Typ Max		Units	Conditions			
V _{OH} Output HIGH Voltage			2.5			V	$I_{OH} = -1 \text{ mA}$	$V_{IN} = V_{IL}$ (Min) or	
		2.0			$I_{OH} = -15 \text{ mA}$		V _{IH} (Max)		
V _{OL}	Output LOW Voltage				0.55	V	I _{OL} = 64 mA	$V_{IN} = V_{IL}$ (Min) or	
					0.50		$I_{OL} = 24 \text{ mA}$	V _{IH} (Max)	
V _{IH}	Input HIGH Voltage	ECL Inputs	-1165		-870	mV	0		
		OE TTL	2.0			V	Guaranteed HIGH Signal for All Inputs		
V _{IL}	Input LOW Voltage	ECL Inputs	-1830		-1475	mV			
		OE TTL			0.8	V	Guaranteed LOW Signal for All Inputs		
I _{BVI}	Input Breakdown Current				10	μΑ	V _{BI} = 7.0V		
I _{IH}	ECL Input HIGH Current	ECL Inputs			240	μА	V V (M-2)		
		OE ECL			350		V _{IN} = V _{IH} (Max)		
	TTL Input HIGH Current	OE TTL			5.0	μА	V _{IN} = 2.7V		
I _{IL}	ECL Input LOW Current	ECL Inputs	0.5			μΑ	V _{IN} = V _{IL} (Min)		
	TTL Input LOW Current	OE TTL			-50	μΑ	V _{IN} = 0.5V		
I _{CEX}	Output HIGH Leakage Curre	ent			250	μΑ			
Ios	Output Short-Circuit Current		-100		-225	mA	$V_{OUT} = 0.0V, V_{TTL} = +5.5V$		
I _{OZH}	3-STATE Current Output HIC	GH.			+50	μΑ	$V_{OUT} = +2.7V$		
I _{OZL}	3-STATE Current Output LO	W			-50	μΑ	V _{OUT} = 0.5V		
V _{FCD}	Input Clamp Diode Voltage V _{EE} Power Supply Current				-1.2	V	$I_{IN} = -18 \text{ mA}$		
I _{EE}			-39		-18	mA	Inputs OPEN		
I _{CCH}	V _{TTL} Power Supply Current HIGH				29	mA			
I _{CCL}	V _{TTL} Power Supply Current LOW				65	mA			
I _{CCZ}	V _{TTL} Power Supply Current 3-STATE				49	mA			

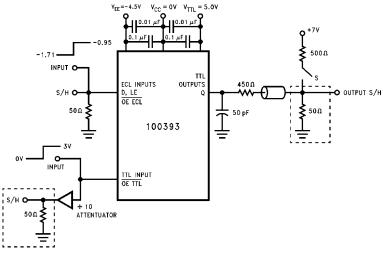
Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

AC Electrical Characteristics

 $V_{EE} = -4.2 V$ to -5.7 V, $V_{CC} = GND$, $V_{TTL} = +4.5 V$ to +5.5 V

Symbol	Parameter	T _C = 0°C		T _C = +25°C		T _C = +85°C		Units	Conditions
Syllibol		Min	Max	Min	Max	Min	Max	Units	Conditions
t _{PLH}	Propagation Delay	2.3	4.8	2.3	4.8	2.3	5.3	ns	Figures 1, 2
t _{PHL}	Data to Output	2.5	4.0	2.3	4.0	2.3	5.5	115	rigules 1, 2
t _{PLH}	Propagation Delay	2.3	5.6	2.3	5.6	2.3	6.4	ns	Figures 1, 2
t _{PHL}	LE to Output	2.5	5.0	2.5	5.0	2.5	0.4		
t _{PZH}	Output Enable Time	2.0	5.5	2.0	5.5	2.0	5.5	ns	Figure 3
t _{PZL}	OE TTL ↓ to Q _N	3.5	8.0	3.5	8.0	3.5	8.0		
t _{PHZ}	Output Disable Time	2.0	6.0	2.0	6.0	2.0	6.0	ns	Figure 3
t _{PLZ}	OE TTL ↑ to Q _N	2.0	5.5	2.0	5.0	2.0	5.0		
t _{PZH}	Output Enable Time	2.4	5.6	2.4	5.6	2.4	5.6	ns	Figure 4
t _{PZL}	OE ECL ↑ to Q _N	3.2	8.5	3.2	8.5	3.2	8.5		
t _{PHZ}	Output Disable Time	2.4	6.0	2.4	6.0	2.4	6.0	ns	Figure 4
t _{PLZ}	OE ECL ↓ to Q _N	3.2	7.6	3.2	7.6	3.2	7.6		
t _S	Setup Time, D _N to LE	0.7		0.7		0.7		ns	Figures 1, 2
t _H	Hold Time, D _N to LE	1.3		1.3		1.3		ns	Figures 1, 2
t _{PW} (L)	Pulse Width LOW, LE	2.0		2.0		2.0		ns	Figures 1Figure 2

Test Circuit



Switch Positions for Parameter Testing

Parameter	S-Position	
t _{PLH} , t _{PHL}	Open	
t _{PHZ} , t _{PZH}	Open	
t_{PLZ}, t_{PZL}	Open	

FIGURE 1. AC Test Setup

Switching Waveforms

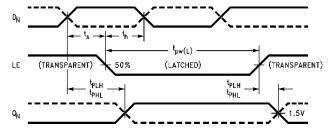


FIGURE 2. Propagation Delays, Setup and Hold Times, and Pulse Width

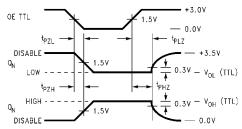


FIGURE 3. Enable and Disable Waveforms, $\overline{\text{OE}}\ \overline{\text{TTL}}$

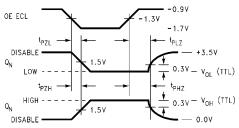
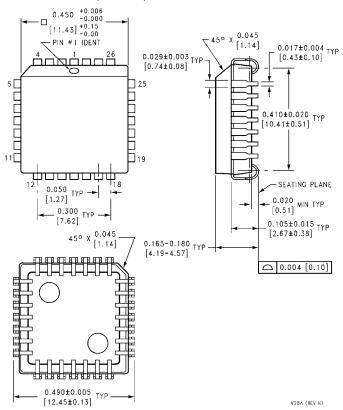


FIGURE 4. Enable and Disable Waveforms, $\overline{\text{OE}}\ \overline{\text{ECL}}$

Physical Dimensions inches (millimeters) unless otherwise noted



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A

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